

Abstract of the Disclosure:

A method for testing a semiconductor memory having a plurality of memory banks involves information being written to memory addresses and/or being read from the memory addresses. The
5 method which logically combines parallel memory bank actuation of the memory addresses using an interleaved mode, which is implemented in relation to disjunct subareas of the memory banks, with one another. This shortens the test time required for testing the semiconductor memory.

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